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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,800	06/28/2003	Chih-Hsin Wang	2003-1	6861
7590	01/10/2005		EXAMINER	
Chih-Hsin Wang 6585 Gillis Dr. San Jose, CA 95120			TRAN, MAI HUONG C	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,800	WANG, CHIH-HSIN	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 June 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-35 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>6/28/03</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-35 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 5,115,289 to Hisamoto et al. in view of Cleaves et al. (6,580,124).

Regarding to claims 1-20, Hisamoto discloses a nonvolatile memory device comprising a substrate 10 of a semiconductor material having a first conductivity type; a semiconductor block 100 over the substrate 10 and having a first sidewall and a second sidewall opposite to each other and a top between first sidewall and second sidewall, the semiconductor block 100 including a first region 40 (source) having a second conductivity type, a second region 50 (drain) having a second conductivity type, and a third region (channel: col. 6, line 45) between the first region and the second region and having first conductivity type; a folded floating gate 30 over the third region of the semiconductor block, the folded floating gate having a first section 30 adjacent first sidewall of the semiconductor block, a second section 30 adjacent the second sidewall of

the semiconductor block, and a third section 30 adjacent the top of the semiconductor block 100 (col. 6, lines 31-53, col. 7, lines 9-23, and fig. 1).

However, Hisamoto does not disclose a control gate disposed over the third section of the folded floating gate. Cleaves et al. teach a control gate disposed over the third section of the folded floating gate as set forth in col. 9, lines 18-27, and fig. 2q.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a control gate disposed over the third section of the folded floating gate in order to form a nonvolatile memory device which can be easily fabricated in a dense array, so that large amounts of data can be stored in a nonvolatile manner (col. 1, lines 25-27).

Regarding to claims 21-30, Hisamoto discloses a nonvolatile memory device comprising a substrate 10 of a semiconductor material having a first conductivity type; a plurality of semiconductor blocks 100 over the substrate 10, each having a first sidewall and a second sidewall and a top between first sidewall and second sidewall, each of the plurality of semiconductor blocks 100 further including a first region 40 (source) of a second conductivity type, a second region 50 (drain) of second conductivity type, and a third region (channel: col. 6, line 45) between the first region and the second region and of first conductivity type; a plurality of folded floating gate 30, each over the third region of a corresponding one of the plurality of semiconductor blocks, and having a first section 30, a second section 30, and a third section 30 adjacent first sidewall, second

sidewall, and the top, respectively, of the corresponding semiconductor block 100 (col. 6, lines 31-53, col. 7, lines 9-23, and fig. 1).

However, Hisamoto does not disclose a plurality of control gates disposed over the plurality of folded floating gate. Cleeves et al. teach a plurality of control gates disposed over the plurality of folded floating gate as set forth in col. 9, lines 18-27, and fig. 2q.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a plurality of control gates disposed over the plurality of folded floating gate in order to form a nonvolatile memory device which can be easily fabricated in a dense array, so that large amounts of data can be stored in a nonvolatile manner (col. 1, lines 25-27).

Regarding to claims 31-35, Hisamoto et al. discloses a nonvolatile memory array comprising a semiconductor substrate 10, a plurality of semiconductor stripes 100 over the substrate substantially parallel to one another, each having a first sidewall and a second sidewall, and a top between first sidewall and second sidewall, each of plurality of stripes further including a plurality of sequentially arranged cells, each cell including a source region 40, a drain region 50, and a channel region there between; a plurality of folded floating gates 30 arranged in a plurality of rows and a plurality of columns, each over the channel region in a corresponding cell and having a first section, a second section, and a third section adjacent first sidewall, second sidewall, and the top, respectively of a corresponding stripe (col. 6, lines 31-53, col. 7, lines 9-23, and fig. 1).

However, Hisamoto does not disclose a plurality of control gates, each disposed over a row of plurality of folded floating gates. Cleeves et al. teach a plurality of control gates, each disposed over a row of plurality of folded floating gates (col. 9, lines 18-27, and fig. 2q).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a plurality of control gates, each disposed over a row of plurality of folded floating gates in order to form a nonvolatile memory device which can be easily fabricated in a dense array, so that large amounts of data can be stored in a nonvolatile manner (col. 1, lines 25-27).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.


Mai-Huong Tran

